> The semiconductor body defines an isolation trench having sidewalls and upper and lower portions, and *encircling an area of the semiconductor body* which contains a semiconductor structure which is to be electrically isolated from other semiconductor structures contained within the semiconductor body but not located within the encircled area. (Emphasis added).

(See page 4, line 25 to page 5, line 4).

Further, the specification describes an example of process steps for defining and etching the isolation trench as follows:

> FIG. 4 ... and FIG. 5 ... show the process continuing with a layer of a suitable mask material 18, such as a photoresist, deposited over the top surface 11A of layer 11 as shown to overlie the regions in which pairs of transistors are to be formed between the storage trenches 12 as previously described. An opening in the mask layer 18 leaves unmasked a central region 19 between trenches 12 of the middle row of memory cells as well as openings around all portions of mask material 18 (as shown as dashed line rectangles in FIG. 4).

(See page 13, lines 15-23). As Fig. 4 shows, the portions of mask material 18 may be strips that cover part of the silicon dioxide layer 16 that is atop storage trenches 12, as well as cover the source and drain regions 40,42, leaving the areas of the semiconductor body that *enclose* the portions of mask material 18 exposed. The specification further describes:

> With the photoresist 18 and the silicon dioxide layers 16 as a mask, there is then etched, typically by anisotropic RIE, the exposed portion of PAD layer 11 and the underlying, now unprotected silicon between the silicon dioxide layers 16.

(See page 13, line 24 to page 14, line 2). The etching step thus removes the portion of PAD layer 11 and the underlying, unprotected silicon that *enclose* the strips of mask material 18 and that *enclose* the storage trenches 12 that are beneath the silicon dioxide layers 16. As a result:

> After such etching, the photoresist mask 18 is removed with the result shown in FIG. 6, where there is shown an isolation trench 20 formed in the semiconductor body 10 where not protected either by the photoresist layer 18 or by the silicon dioxide regions 16 deposited from TEOS. This isolation trench 20 is self aligned to the sidewall edges of the deep storage trenches 12 also exists between rows of memory cells .... .

(See page 14, lines 3-9).

The above-cited portion of the specification relates to an embodiment which shows a portion of the isolation trench 20 that is between two of the storage trenches 12. Further, the isolation trench 20 is formed in *all* of the unprotected regions, as shown in Fig. 4, and *encloses* the area of the semiconductor body that was protected by the photoresist 18 and the silicon dioxide layers 16. Clearly, the limitation "an isolation trench enclosing an area of the semiconductor body" is described in the specification and drawings.

The Examiner also asserts that "In claim 1, the phrase 'a lower portion that is in electrical contact with the semiconductor body at the bottom of the isolation trench' is not described in the specification and drawings." However, Figs. 9-11 clearly show a p+ polysilicon layer 26 that is formed in the isolation trench 20 and which contacts the p+ region 23 of the semiconductor body at the bottom of the isolation trench 20, thereby providing electrical contact between a lower portion 26A of the p+ polysilicon layer and the semiconductor body. (See also, page 14, lines 23 – page 15, line 10 of the specification.) Clearly, the limitation is supported by the specification and drawings.

It is therefore submitted that the claims are in compliance with the requirements of 35 U.S.C. § 112.

Turning to the art rejections, claims 1-2 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wada (U.S. Patent No. 6,274,919 B1). It is submitted, however, that the claims are patentably distinguishable over Wada.

The Wada patent shows, in Figs. 2B-2D, a trench isolated device in which all of the walls of a trench 12, as well as the bottom of a trench, are lined with an insulator film 23. A polycrystalline silicon deposit 24 "fills the entire cavity space of the trenches 12", i.e., the remainder of the trench is filled with polycrystalline silicon 24. (See column 4, line 59- column 5, line 12).

The Examiner does not assert that Wada discloses an electrically conductive material having a lower portion that is in an electrical contact with the semiconductor body at the bottom of the isolation trench. Rather, the Examiner argues that this limitation is not described in the specification and drawings. However, for the reasons described above, the disclosure clearly provides support for these features. In contrast, Wada does not disclose or suggest such features. Instead, Wada shows an insulator film 23 that covers the bottom of the trench 12 and *electrically isolates* the polycrystalline silicon 24 from the substrate 7 and thereby *prevents* electrical contact with the semiconductor body.

It follows that Wada does not suggest:

> the lower portion of the isolation trench being at least partly filled with an electrically conductive material that has sidewall portions which are at least partly separate from the sidewalls of the lower portion of the isolation trench by a first electrical insulator, said electrically conductive material having a lower portion that is in electrical contact with the semiconductor body at the bottom of said isolation trench

as called for in claim 1.

The Examiner also incorrectly argues that the upper portion of the isolation trench is filled with a second electrical insulator and refers to gate insulator film 9 shown in Fig. 2D of Wada. However, as described above, the polycrystalline silicon deposit 24 *completely fills* the trench. The insulator film 9 is formed *atop* that polycrystalline silicon deposit 24 that completely fills the trench, and thus the insulator film is formed *above the* trench and does not fill an upper portion of the trench.

Wada does not suggest:

> the upper portion of the isolation trench being filled with a second electrical insulator.

as defined in claim 1.

Wada therefore does not suggest the combination defined in claim 1 and does not anticipate the claim.

Claim 2 depends from claim 1 and further defines and limits the invention set out in the independent claim as well as calls for additional limitations. It follows that claim 2 likewise defines a combination that is patentably distinguishable over Wada.

Accordingly, the withdrawal of the rejection of claims 1-2 under 35 U.S.C. § 102 is respectfully requested.

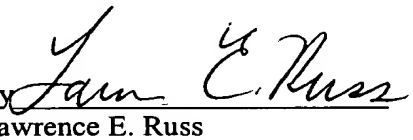
In view of the foregoing remarks and the amendments herein, it is submitted that the rejection of the claims under 35 U.S.C. §§ 102 and 112 are overcome.

It is therefore submitted that this case is in condition for allowance and such action is respectfully requested. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that the Examiner telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which the Examiner might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: October 14, 2002

Respectfully submitted,

By 

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